WHAT IS CLAIMED IS:

1. A method for aligning and inserting data elements into a memory based upon an instruction sequence consisting of one or more alignment instructions and a single store instruction, comprising the steps of:

given a data item that includes a data element to be stored,

aligning the data element in another memory with respect to a predetermined position in the memory, in response to the one or more alignment instructions;

dynamically generating a mask to enable writing of memory bit lines that correspond to the aligned data element; and

writing the memory bit lines to the memory under a control of the mask, wherein said generating and writing steps are performed in response to the single store instruction.

2. The method of claim 1, wherein the other memory is a register.

3. The method of claim 1, further comprising the step of computing the mask from an address argument corresponding to the single store instruction.

4. The method of claim 3, wherein the address argument comprises a displacement value and an address value.

5. The method of claim 4, wherein the address value specifies a particular register.

6. The method of claim 1, further comprising the step of computing the mask based upon a data type of the data element.

7. The method of claim 1, wherein the predetermined position in the memory corresponds to a target position within a memory line.

8. The method of claim 1, further comprising the step of computing and checking parity information corresponding to the data element.

9. The method of claim 1, further comprising the step of computing and checking error correction code (ECC) information corresponding to the data element.

10. The method of claim 1, further comprising the step of intermediately storing the memory bit lines from the other memory to a read-write buffer before said writing step.

11. The method of claim 1, wherein the instruction sequence is without a merge instruction.

12. A system for aligning and inserting data elements into a memory in response to an instruction sequence consisting of one or more alignment instructions and a single store instruction, comprising:

means for receiving a data item that includes a data element to be stored;

means for aligning the data element in another memory with respect to a predetermined position in the memory, in response to the one or more alignment instructions;

means for dynamically generating a mask to enable writing of memory bit lines that correspond to the aligned data element, in response to the single store instruction; and

means for writing the memory bit lines to the memory under a control of the mask, in response to the single store instruction.

13. The system of claim 12, wherein said system exploits partial line write capabilities of the memory.

14. The system of claim 12, further comprising logic for computing and checking parity information corresponding to the data element.

15. The system of claim 12, further comprising logic for computing and checking error correction code (ECC) information corresponding to the data element.

16. The system of claim 12, further comprising:

a CPU;

a read-write buffer for intermediately storing, under a control of the CPU, the memory bit lines from the other memory before said writing step.

17. The system of claim 12, wherein the memory comprises a cache, and said means for writing writes the data element to the cache under the control of the mask.

18. The system of claim 12, wherein the data item is a data word.

19. A method for storing data in a memory based upon an instruction sequence consisting of one or more alignment instructions and a single store instruction, comprising the steps of:

aligning the data in a register relative to a location of the data within a target memory address line, in response to the one or more alignment instructions; and

storing a portion of the aligned data within the memory under a control of data type information and an address argument specified by the single store instruction, in response to the single store instruction.

20. The method of claim 19, wherein said storing step stores the portion of the aligned data under the control of a write mask computed from the data type information and the address specified by the single store instruction.

21. The method of claim 19, further comprising the step of intermediately storing the aligned data from the register to a read-write buffer before said storing step.

22. The method of claim 19, wherein the address argument comprises a displacement value and an address value.

23. The method of claim 22, wherein the address value specifies a particular register.

24. The method of claim 19, wherein the instruction sequence is without a merge instruction.

25. In a memory system with a register and a memory and without an alignment network, a method for storing data in the memory based upon a single store instruction, the method comprising the steps of:

generating memory write instructions for directly storing a plurality of bits from the register to a memory line in the memory under a control of a mask, a bit range of the plurality of bits being specified by parameters of the single store instruction.

26. The method of claim 25, wherein the single store instruction includes a type specifier that indicates a number of bits to be stored, and said method further comprises the step of extracting the number of bits to be stored from the type specifier included in the single store instruction.

27. The method of claim 25, wherein the single store instruction includes an operand that indicates a number of bits to be stored, and said method further comprises the step of extracting the number of bits to be stored from the operand included in the single store instruction.

28. The method of claim 25, wherein the single store instruction includes an operand at at least one of a start position and an end position of the bit range, and said

method further comprises the step of extracting the operand included in the single store instruction.

29. The method of claim 25, wherein at least one of a start position and an end position of the bit range is indicated by a memory address operand included in the single store instruction, and said method further comprises the step of extracting the at least one of the start position and the end position of the bit range from the memory address operand included in the single store instruction.